What is claimed is:

1. A synchronous flash memory device comprising:
a first memory array with a first memory array dimensionality;
a control circuit;
a synchronous memory interface, wherein the control circuit is adapted to logically adapt the first memory array dimensionality to a second memory array dimensionality; and
wherein the synchronous memory interface is adapted to communicate data on the rising and falling edges of an externally provided clock.

2. The synchronous flash memory device of claim 1, wherein the memory array further comprises a plurality of array banks.

3. The synchronous flash memory device of claim 2, wherein the plurality of array banks each have a first row dimension and a first column dimension, and where the control circuit is adapted to logically adapt the first row dimension and the first column dimension of each array bank to a second row dimension and a second column dimension.

4. The synchronous flash memory device of claim 3, wherein the second row dimension and the second column dimension are the same as a DDR memory device.

5. The synchronous flash memory device of claim 2, wherein each array bank of the plurality of array banks further comprise a plurality of segments.

6. The synchronous flash memory device of claim 5, wherein each array bank of the plurality of array banks comprise four segments.

7. A synchronous non-volatile memory device comprising:

a memory array with a plurality of array banks, each array bank having a first number of rows and a first number of columns;

a synchronous memory interface, wherein, for each array bank of the plurality of array banks, wherein the synchronous memory interface is adapted to logically adapt the first number of rows and the first number of columns to a second number of rows and a second number of columns; and

wherein the synchronous memory interface is adapted to communicate data on a rising edge and a falling edge of an externally provided clock.

8. The synchronous flash memory device of claim 7, wherein the plurality of array banks equal four array banks.

9. The synchronous flash memory device of claim 7, wherein each array bank of the plurality of array banks further comprise a plurality of segments.

10. The synchronous flash memory device of claim 9, wherein the plurality of segments are divided by a row range.

11. The synchronous flash memory device of claim 9, wherein each array bank of the plurality of array banks comprises four segments.

12. The synchronous flash memory device of claim 7, wherein the second number of rows and the second number of columns matches that of a DDR memory.

13. A synchronous flash memory device comprising:

a first memory array with a first memory array dimensionality;

a control circuit, wherein the control circuit is adapted to logically adapt the first

memory array dimensionality to a second memory array dimensionality; and

a synchronous memory interface, wherein the synchronous memory interface comprises,

an address interface,

a data interface,

a control interface, and

wherein the data interface is adapted to communicate data on the rising and falling edges of an externally provided clock.

14. The synchronous flash memory device of claim 13, wherein the address interface further comprises an extended address interface, wherein the extended address interface allows extended access to the synchronous flash memory device.

15. The synchronous flash memory device of claim 14, wherein the extended address interface further allows access to the first memory dimensionality.

16. A synchronous flash memory device comprising:

a first memory array with a plurality of array banks, each having a first row dimension and a first column dimension;

a control circuit, wherein the control circuit is adapted to logically adapt the first row dimension and the first column dimension of each of the plurality of banks to a second row dimension and a second column dimension;

a synchronous memory interface, wherein the synchronous memory interface comprises,

an address interface,

an extended address interface,

a data interface, and

a control interface; and

wherein the synchronous memory interface is adapted to communicate data on the rising and falling edges of an externally provided clock.

17. The synchronous flash memory device of claim 16, wherein the extended address interface is adapted to allow access to the first row dimension.

18. The synchronous flash memory device of claim 16, wherein the extended address interface is adapted to allow access to the first column dimension.

19. The synchronous flash memory device of claim 16 wherein the extended address interface further comprises an additional address interface is adapted to allow access to the first row dimension of the synchronous flash memory device.

20. The synchronous flash memory device of claim 19, wherein the additional address interface has two address lines and is adapted to allow access into the first row dimension of the synchronous flash memory device.

21. The synchronous flash memory device of claim 16, wherein the plurality of array banks further comprise a plurality of segments, and wherein the extended address interface further comprises an additional address interface adapted to select a segment of an active bank of the synchronous flash memory device.

22. The synchronous flash memory device of claim 21, wherein the additional address interface has two address lines is adapted to allow selection of the segment of the active bank of the synchronous flash memory device.

23. The synchronous flash memory device of claim 21, wherein the additional address interface is adapted to allow associating an active row of a selected segment with any other segment in the active bank of the synchronous flash

memory device.

24. A method of operating a synchronous non-volatile memory device comprising:
dividing a memory array with a first memory array dimensionality into a plurality of sections;
logically adapting the plurality of sections of the memory array to form an emulated virtual second memory array dimensionality; and
communicating data on the rising and falling edges of an externally provided clock.

25. The method of claim 24, wherein dividing the memory array into a plurality of sections further comprises dividing the memory array into a plurality of array banks.

26. The method of claim 25, wherein dividing the memory array into the plurality of array banks further comprises dividing the memory array into a plurality of array banks such that the array banks have a first row dimension and a first column dimension.

27. The method of claim 26, wherein logically adapting the plurality of sections of the memory array to form the emulated virtual second memory array dimensionality further comprise logically adapting the first row dimension and the first column dimension of each array bank to a second row dimension and a second column dimension.

28. The method of claim 27, wherein logically adapting the first row dimension and the first column dimension of each array bank to a second row dimension and a second column dimension further comprise logically adapting the first row dimension and the first column dimension of each array bank to a second row

dimension and a second column dimension, where the second row dimension and the second column dimension are the same as a DDR memory device.

29. The method of claim 25, wherein dividing the memory array into the plurality of array banks further comprises dividing each array bank into a plurality of segments.

30. A method of operating a synchronous flash memory device comprising:

dividing a memory array with a first memory array dimensionality into a plurality of array banks;

dividing each array bank of the plurality of array banks into a plurality of segments;

logically adapting the plurality of array banks and plurality of segments of the first memory array dimensionality of the memory array to form an emulated virtual second memory array dimensionality, wherein accessing the emulated virtual second memory array dimensionality occurs through a synchronous memory interface on the rising and falling edges of a clock signal; and

allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal.

31. The method of claim 30, wherein allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal further comprises allowing access to the first row dimension of each array bank through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal.

32. The method of claim 30, wherein allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal further comprises allowing access to the first column dimension of each array bank of the plurality of array banks through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal.

33. The method of claim 31, wherein allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal further comprising allowing access to the first memory array dimensionality of the memory array through the synchronous memory interface and an extended interface on the rising and falling edges of the clock signal, where an additional address interface of the extended interface allows selection of a segment of an active bank of the synchronous flash memory device.

34. The method of claim 33, wherein the additional address interface allows associating an active row of a selected segment with any other segment in the active bank of the synchronous flash memory device.

35. A method of logically mapping a synchronous non-volatile memory device comprising:

dividing each bank of a first plurality of banks in a first memory array into a plurality of segments;

logically mapping the plurality of segments to appear as a second memory array with a second plurality of segments; and

communicating data from the second memory array on the rising and falling edges of an externally provided clock.

36. A system comprising:

a synchronous memory controller; and

a synchronous flash memory device, wherein the synchronous flash memory device comprises,

a memory array with a first memory array dimensionality,

a control circuit,

a synchronous memory interface,

wherein the control circuit is adapted to logically adapt the first memory array dimensionality to a second memory array dimensionality, and

wherein the synchronous memory interface is adapted to transfer data on the rising and falling edges of an externally provided clock.

37. The system of claim 36, wherein the synchronous memory controller further comprises one of a processor, an ASIC, and an FPGA.